



### 256Kx8 Monolithic SRAM

#### FEATURES

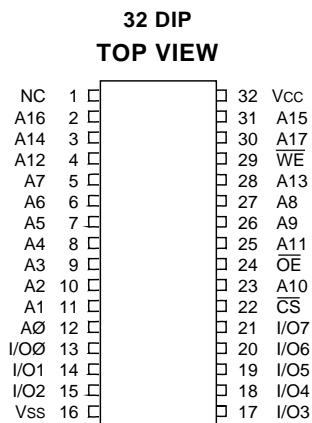
- Access Times of 20, 25, 35, 45, 55ns
- Data Retention Function (LPA Versions)
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks
- Organized as 256Kx8
- Commercial, Industrial and Military Temperature Ranges
- JEDEC Approved Evolutionary Pinout
  - 32 pin Ceramic DIP, 0.6 mils wide (Package 9)
- Single +5V ( $\pm 10\%$ ) Supply Operation

The EDI88257CA is a 2 Megabit 256Kx8 bit Monolithic CMOS Static RAM.

The 32 pin DIP pinout adheres to the JEDEC evolutionary standard for the two megabit device. The device is upgradeable to the 512Kx8 SRAM, the EDI88512CA. Pin 1 becomes the higher order address.

A Low Power version, EDI88257LPA, offers a data retention function for battery back-up operation. Military product is available compliant to Appendix A of MIL-PRF-38535.

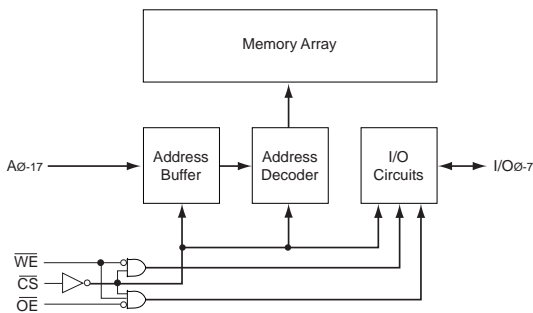
**FIG. 1 PIN CONFIGURATION**



#### PIN DESCRIPTION

I/O0-7	Data Inputs/Outputs
A0-17	Address Inputs
WE	Write Enable
CS	Chip Selects
OE	Output Enable
Vcc	Power (+5V $\pm 10\%$ )
Vss	Ground
NC	Not Connected

#### BLOCK DIAGRAM





**ABSOLUTE MAXIMUM RATINGS**

Parameter		Unit
Voltage on any pin relative to Vss	-0.5 to 7.0	V
<b>Operating Temperature TA (Ambient)</b>		
Industrial	-40 to +85	°C
Military	-55 to +125	°C
Storage Temperature, Ceramic	-65 to +150	°C
Power Dissipation	1.5	W
Output Current	20	mA
Junction Temperature, TJ	175	°C

**NOTE:**

Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**CAPACITANCE**

(TA = +25°C)

Parameter	Symbol	Condition	Max	Unit
Address Lines	C1	VIN = Vcc or Vss, f = 1.0MHz	12	pF
Input/Output Lines	Co	VOUT = Vcc or Vss, f = 1.0MHz	14	pF

These parameters are sampled, not 100% tested.

**DC CHARACTERISTICS**

(VCC = 5V, TA = +25°C)

Parameter	Symbol	Conditions	Min Typ Max			Units
			Min	Typ	Max	
Input Leakage Current	ILI	VIN = 0V to Vcc	-10	—	+10	µA
Output Leakage Current	ILO	VIO = 0V to Vcc	-10	—	+10	µA
Operating Power Supply Current	Icc1	WE, CS = VIL, IIO = 0mA, Min Cycle (20-25ns) (35-55ns)	—	—	225	mA
			—	—	200	mA
Standby (TTL) Power Supply Current	Icc2	CS ≥ VIH, VIN ≤ VIL, VIN ≥ VIH	—	—	60	mA
Full Standby Power Supply Current	Icc3	CS ≥ Vcc -0.2V VIN ≥ Vcc -0.2V or VIN ≤ 0.2V	CA	—	25	mA
			LPA	—	20	mA
Output Low Voltage	VOL	IOL = 8.0mA	—	—	0.4	V
Output High Voltage	VOH	IOH = -4.0mA	2.4	—	—	V

NOTE: DC test conditions: VIL = 0.3V, VIH = Vcc -0.3V

**TRUTH TABLE**

OE	CS	WE	Mode	Output	Power
X	H	X	Standby	High Z	Icc2, Icc3
H	L	H	Output Deselect	High Z	Icc1
L	L	H	Read	Data Out	Icc1
X	L	L	Write	Data In	Icc1

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Supply Voltage	Vss	0	0	0	V
Input High Voltage	VIH	2.2	—	Vcc +0.5	V
Input Low Voltage	VIL	-0.3	—	+0.8	V



**AC CHARACTERISTICS – READ CYCLE**

(V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol		20ns		25ns		35ns		45ns		55ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tAVAV	tRC	20		25		35		45		55		ns
Address Access Time	tAVOQ	tAA		20		25		35		45		55	ns
Chip Select Access Time	tELOQ	tACS		20		25		35		45		55	ns
Chip Select to Output in Low Z (1)	tELOX	tCLZ	3		3		3		3		3		ns
Chip Disable to Output in High Z (1)	tEHOZ	tCHZ	0	8	0	10	0	15	0	20	0	20	ns
Output Hold from Address Change	tAVOQ	tOH	0		0		0		0		0		ns
Output Enable to Output Valid	tGLOV	tOE		10		12		15		25		25	ns
Output Enable to Output in Low Z (1)	tGLOX	tOLZ	0		0		0		0		0		ns
Output Disable to Output in High Z (1)	tGHOZ	tOHZ	0	8	0	10	0	15	0	20	0	20	ns

1. This parameter is guaranteed by design but not tested.

**AC CHARACTERISTICS – WRITE CYCLE**

(V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol		20ns		25ns		35ns		45ns		55ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	20		25		35		45		45		ns
Chip Select to End of Write	tELWH tELEH	tCW tCW	15 15		17 17		25 25		30 30		30 30		ns ns
Address Setup Time	tAVWL tAVEL	tAS tAS	0 0		0 0		0 0		0 0		0 0		ns ns
Address Valid to End of Write	tAVWH tAVEH	tAW tAW	15 15		17 17		25 25		30 30		30 30		ns ns
Write Pulse Width	tWLWH tWLEH	tWP tWP	15 15		17 17		25 25		30 30		30 30		ns ns
Write Recovery Time	tWHAX tEHAX	tWR tWR	0 0		0 0		0 0		0 0		0 0		ns ns
Data Hold Time	tWHDX tEHDX	tDH tDH	0 0		0 0		0 0		0 0		0 0		ns ns
Write to Output in High Z (1)	tWLOZ	tWHZ	0	8	0	10	0	25	0	30	0	30	ns
Data to Write Time	tDVWH tDVEH	tDW tDW	10 10		12 12		20 20		25 25		25 25		ns ns
Output Active from End of Write (1)	tWHQX	tWLZ	0		0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

**AC TEST CONDITIONS**

Figure 1

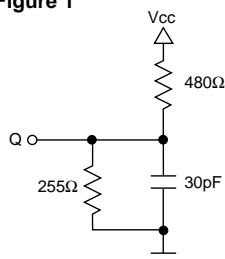
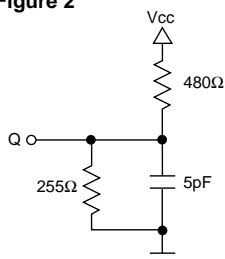


Figure 2

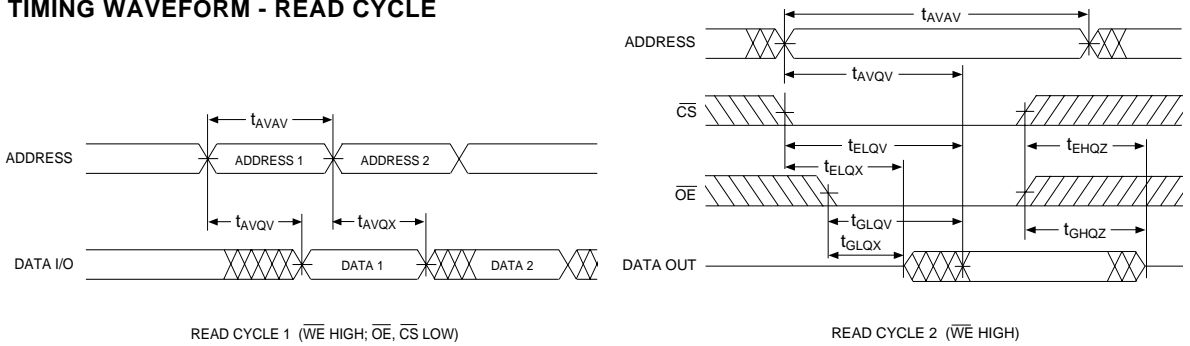


Input Pulse Levels	V <sub>SS</sub> to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

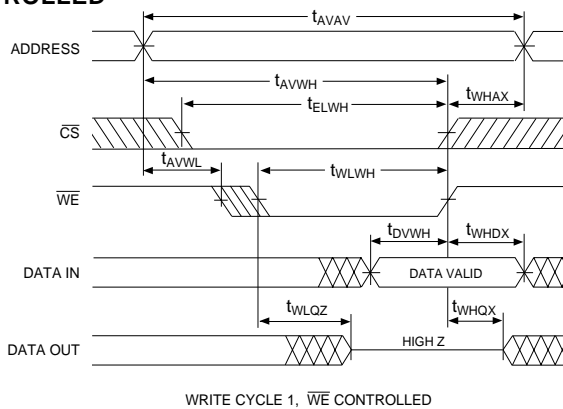
NOTE: For tEHOZ, tGHOZ and tWLOZ, CL = 5pF Figure 2)



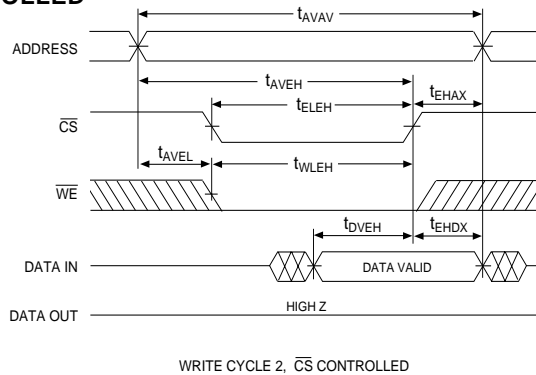
**FIG. 2**  
**TIMING WAVEFORM - READ CYCLE**



**FIG. 3**  
**WRITE CYCLE -  $\overline{WE}$  CONTROLLED**



**FIG. 4**  
**WRITE CYCLE -  $\overline{CS}$  CONTROLLED**

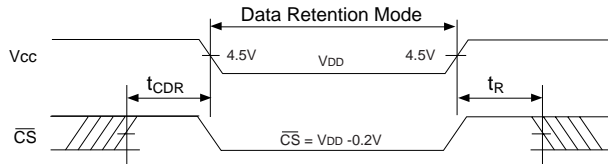




**DATA RETENTION CHARACTERISTICS (EDI88257LPA ONLY)**  
(TA = -55°C to +125°C)

Characteristic Low Power Version only	Sym	Conditions	Min	Typ	Max	Units
Data Retention Voltage	V <sub>DD</sub>	V <sub>DD</sub> = 2.0V	2	-	-	V
Data Retention Quiescent Current	I <sub>CCDR</sub>	$\overline{CS} \geq V_{DD} - 0.2V$	-	-	2	mA
Chip Disable to Data Retention Time	T <sub>CDR</sub>	V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V	0	-	-	ns
Operation Recovery Time	T <sub>R</sub>	or V <sub>IN</sub> ≤ 0.2V	T <sub>AVAV</sub>	-	-	ns

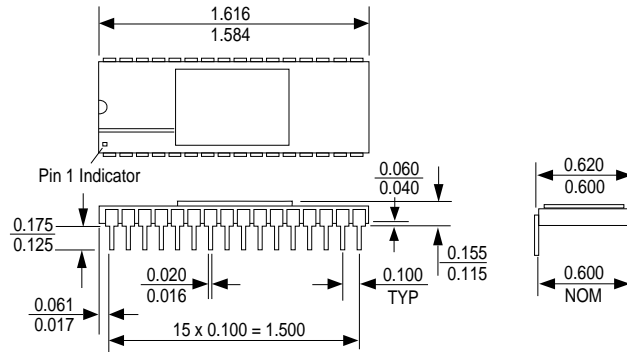
**FIG. 5**  
**DATA RETENTION -  $\overline{CS}$  CONTROLLED**



DATA RETENTION,  $\overline{CS}$  CONTROLLED



PACKAGE 9: 32 PIN SIDEBRAZED CERAMIC DIP (600mils wide)



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

EDI 8 8 257 CA X X X

WHITE ELECTRONIC DESIGNS

SRAM

ORGANIZATION, 256Kx8

TECHNOLOGY:

CA = CMOS Standard Power

LPA = Low Power

ACCESS TIME (ns)

PACKAGE TYPE:

C = 32 lead Sidebrazed DIP, 600 mil (Package 9)

DEVICE GRADE:

B = MIL-STD-883 Compliant

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C